List of Claims:

Claims 1-21 (cancelled)

Claim 22 (new): A method of protecting a peripheral region while forming a self-aligned gate in a core region, said method comprising the steps of:

fabricating a dielectric layer interrupted by trenches filled with insulating material in a silicon substrate to form a structure, wherein said structure includes said peripheral region and said core region;

depositing a polysilicon layer on said dielectric layer and said insulating material;

forming a protective mask layer on said polysilicon layer over an area of said peripheral region; and

applying polysilicon polishing to said polysilicon layer and said protective mask layer.

Claim 23 (new): The method of claim 22, wherein said protective mask layer comprises silicon dioxide.

Claim 24 (new): The method of claim 22, wherein said protective mask layer comprises silicon nitride.

Claim 25 (new): The method of claim 22, wherein said area of said peripheral region substantially covers an active portion of said peripheral region.

Claim 26 (new): The method of claim 25, wherein said area is defined by a photomask obtained by shrinking a feature size in said peripheral region.

Claim 27 (new): The method of claim 22, wherein said area of said peripheral region substantially covers said peripheral region.

Claim 28 (new): The method of claim 27, wherein said area is defined by a photomask having an opening window for said core region.

Claim 29 (new): The method of claim 22, wherein said core region is a flash memory circuit.

Claim 30 (new): The method of claim 22 further comprising the steps of:

depositing an ONO layer on said structure after said applying polysilicon polishing step;

masking said core region; and

etching said remaining polysilicon layer in said peripheral region.

Claim 31 (new): An integrated circuit structure comprising:

a dielectric layer interrupted by trenches filled with insulating material in a silicon substrate, wherein said structure includes said peripheral region and said core region;

a polysilicon layer on said dielectric layer and said insulating material;

a protective mask layer on said polysilicon layer over an area of said peripheral region; and

wherein said protective mask protects said peripheral region during polysilicon polishing of said structure.

Claim 32 (new): The integrated circuit structure of claim 31, wherein said protective mask layer comprises silicon dioxide.

Claim 33 (new): The integrated circuit structure of claim 31, wherein said protective mask layer comprises silicon nitride.

Claim 34 (new): The integrated circuit structure of claim 31, wherein said area of said peripheral region substantially covers an active portion of said peripheral region.

Claim 35 (new): The integrated circuit structure of claim 34, wherein said area is defined by a photomask obtained by shrinking a feature size in said peripheral region.

Claim 36 (new): The integrated circuit structure of claim 31, wherein said area of said peripheral region substantially covers said peripheral region.

Claim 37 (new): The integrated circuit structure of claim 36, wherein said area is defined by a photomask having an opening window for said core region.

Claim 38 (new): An integrated circuit fabricated using a method of protecting a peripheral region while forming a self-aligned gate in a core region, said method comprising the steps of:

fabricating a dielectric layer interrupted by trenches filled with insulating material in a silicon substrate to form a structure, wherein said structure includes said peripheral region and said core region;

depositing a polysilicon layer on said dielectric layer and said insulating material;

forming a protective mask layer on said polysilicon layer over an area of said peripheral region; and

applying polysilicon polishing to said polysilicon layer and said protective mask layer.

Claim 39 (new): The integrated circuit of claim 38, wherein said area of said peripheral region substantially covers an active portion of said peripheral region.

Claim 40 (new): The integrated circuit of claim 38, wherein said area of said peripheral region substantially covers said peripheral region.

Claim 41 (new): The integrated circuit of claim 38, wherein said method further comprising the steps of:

depositing an ONO layer on said structure after said applying polysilicon polishing step;

masking said core region; and

etching said remaining polysilicon layer in said peripheral region.